135.1 through 135.M. In one embodiment, memory system 100 has eight memory subsystems [and] each with eight memory devices 135 (i.e. N [plus] times M equals [eight] sixty-four). In another embodiment, memory devices 135 are dynamic random access memory devices (DRAMs). The number of memory devices 135 connected to each buffer register 131 may, however, differ from that shown in memory system 100 without departing from the spirit of the present invention.

The two paragraphs beginning at page 8, line 18 are amended as follows:

Each data register 141 is connected between the plurality of memory devices 135 and data bus 115. For memory read operations, data registers 141 receive and latch data information from memory devices 135. Upon the next clock cycle, data registers 141 provide the information to memory controller 105 by driving the data information on data bus 115. For memory write operations, each data register 141 receives and latches data information from data bus [120] 115. Upon the next clock cycle, data registers 141 drive the data information to their corresponding M memory devices 135. In this manner, the load on data bus [120] 115 is reduced from N*M devices to only N devices.

Each C/A buffer register 131, its corresponding plurality of memory devices 135.1 through 135.M and its corresponding data register 141 define a pipelined memory subsystem 130. Memory subsystems 130.1 through 130.N allow C/A bus 110 and data bus [120] 115 to operate at a significant higher data rate since the loading was reduced by a factor of M. Pipelined memory subsystems 130, however, add a two clock cycle delay to DRAM access. In order to ensure efficient operation, the packet protocol used for communication is defined to incorporate a first delay for C/A buffer register 131 and a second delay for data register 141. Furthermore, memory controller 105 issues command and address packets and data packets in pipeline fashion such that the first delay and the second delay do not have a substantial impact on the performance of memory system 100.

Please add the following paragraph to the specification at page 5, line 21:

Figure 6 is a block diagram of a dynamic random access memory device.